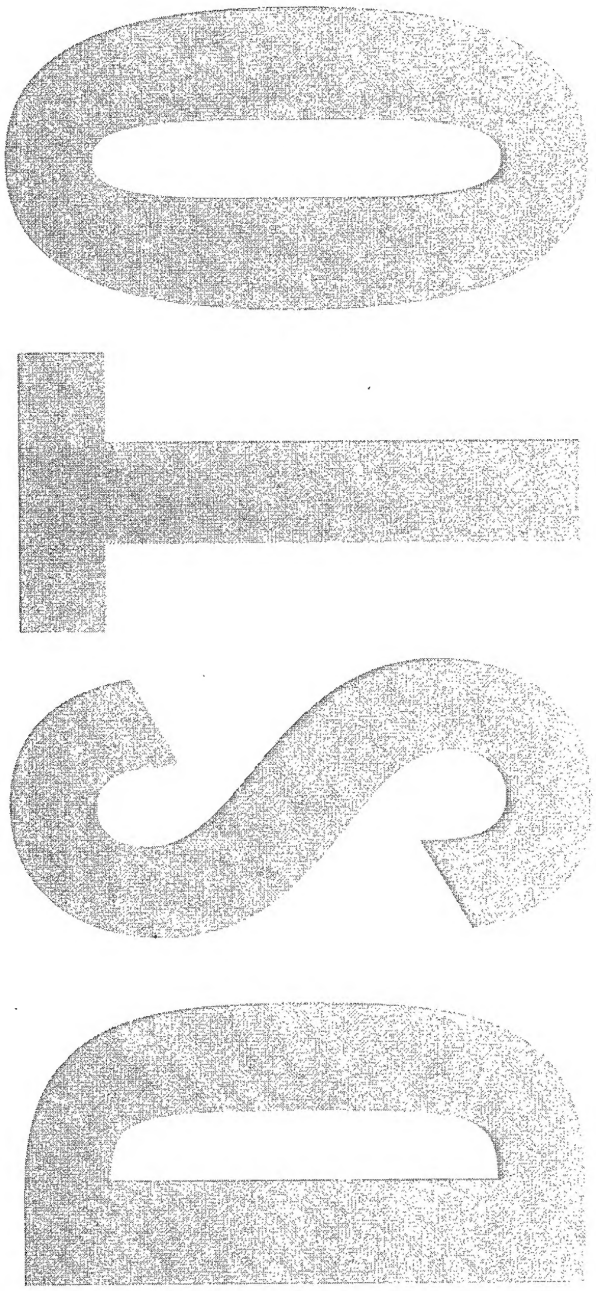

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Air Operations Division
Aeronautical and Maritime Research Laboratory

DSTO-GD-0325

ABSTRACT

A data acquisition system based on commercially available personal computer hardware is described. This system was developed to meet the requirements of the Royal Australian Navy in conduct of flight trials with helicopters operating at sea from ships fitted with helicopter flight decks. All aspects of the system are controlled by software, enabling rapid setup of sample rates, gains, and filter characteristics. Data may be displayed in real-time, and further analysis of recorded data performed post-flight.

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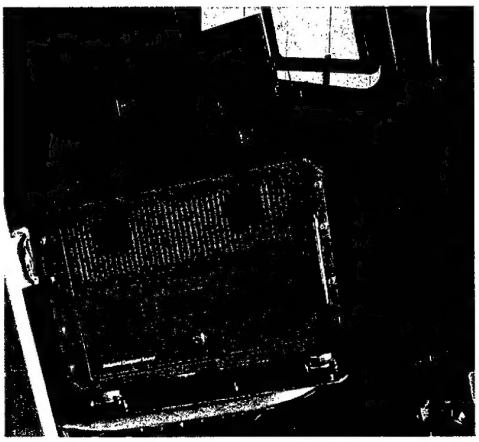
Integrated Data Acquisition System (IDAS)

Executive Summary



Air Operations Division (AOD) of the Aeronautical and Maritime Research Laboratory (AMRL) has been associated with the Royal Australian Navy (RAN) Aircraft Maintenance and Flight Trials Unit (AMAFTU) for many years. At the request of the RAN, an airborne data acquisition system has been developed for use by AMAFTU to record in-flight data from various helicopter types. The system allows data from a range of transducers to be recorded, processed in real-time, and displayed to the pilot (eg the amount of control authority remaining).

Data are used for various investigations, such as the development of a helicopter-ship computer model to simulate the complex interactions between the 'Adelaide' class FFG-7 and the Sikorsky S-70B-2.

To meet both AOD and AMAFTU requirements for trials, an Integrated Data Acquisition System (IDAS) was developed. IDAS follows on from two systems developed in the late 1970s and mid 1980s. These systems, known as the Microprocessor Airborne Data Acquisition and Replay (MADAR), and its successor, the Versatile Airborne Data Acquisition And Replay (VADAR), have been operated successfully by AMAFTU to acquire data from various helicopters and ships. AMAFTU conducts a First of Class Flight Trial (FOCFT) for each helicopter-ship combination in order to establish operational limits. Typically, two IDAS units are used in a FOCFT, one installed in the helicopter to gather flight data such as controls and motion, the other installed aboard the ship to acquire motion and wind data. For the helicopter and ship type combination, the ship helicopter operating limits (SHOLs) for various conditions are determined by later analysis of the data. The value of this work to Australian Defence is that it allows data collection from helicopters operating from ships during adverse weather conditions, the subsequent processing of which will enable the determination of SHOLs.

During 1990 a preliminary FOCFT was conducted with a RAN Seahawk S-70B-2 helicopter operating from an FFG-7 frigate. Since then other FOCFTs have occurred, including an army Black Hawk S-70A-9 helicopter operating from the heavy landing ship HMAS Tobruk and the supply ship HMAS Success.

An important requirement of FOCFTs is that the helicopter be instrumented to record selected data and that the pilot be provided with a calibrated real-time display of instantaneous control positions with respect to fixed limits. In the case of FOCFTs, the test pilot must have a visual indication of available control authority to ensure the safety of the aircrew and aircraft. The Seahawk and Black Hawk helicopters have moveable post-mixed end-stops, and the available pilot control authority is calculated from a number of transducer inputs.

The IDAS system includes a set of "Windows" based applications that enable easy set-up and linearisation of parameters, graphical display of data during acquisition, and comprehensive post-flight analysis.

Authors

J.F.Harvey
Air Operations Division

John Harvey graduated from the Royal Melbourne Institute of Technology in 1964. He commenced employment at the Aeronautical Research Laboratories in 1958. He has worked in several areas, including data acquisition and control systems for wind tunnel research tasks and helicopter flight trials for the Royal Australian Navy. At the time of his retirement in 1999, he was head of the Air Operations Simulation Centre at the Aeronautical and Maritime Research Laboratory.

K.Cameron
Air Operations Division

Keith Cameron obtained a B.Sc. (hon) in aeronautical engineering from the City University London while working for the UK Defence Department. He then studied at the Cranfield Institute of Technology and was awarded a M.Sc. in aerodynamics in 1975. Returning to Australia in 1975 he joined the Department of Transports Flying Unit as a flight operations engineer. He moved to the then Aeronautical Research Laboratory (ARL) in 1976 to partake in remotely piloted aircraft development. During his time at ARL he has worked on systems aspects of a number of projects including Ikara and Nulka. This work has included aerodynamic testing, development of data aquisition systems, autopilot development, trials and studies at both systems and operational levels. This was followed by work in the area of instrumentation and data aquisition systems for aircraft trials and wind tunnels.

M.A.Spataro
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Michael Spataro completed an Honours degree in Electrical and Computer Systems Engineering at Monash University in 1988. He has been employed at the Aeronautical and Maritime Research Laboratory since 1990. He has worked in the areas of electronic design and software development for data acquisition, wind tunnel instrumentation, and motion control. He is currently a Senior Professional Officer, and is involved in Night Vision Goggle research in the Air Operations Simulation Centre.

O.F.Holland
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Owen Holland graduated as an Electronic Engineer from Bendigo College of Advanced Education in 1977 and furthered his studies in Electronic Engineering at the Royal Melbourne Institute of Technology, graduating in 1983. He commenced employment at the Aeronautical Research Laboratory in 1978, where he has worked in the areas of data acquisition for wind tunnels and RAN helicopter flight trials.

F.J.Bird
Air Operations Division

Fred Bird qualified as a Technical Officer after completing 5 years training with the then Postmaster General's Dept Research Laboratories in 1967. In 1969 he joined the then Australian Broadcasting Control Board (ABCB) and worked in RF propagation studies for TV broadcast station planning. He joined ARL in 1985 and retrained in data acquistion system design. This led to work in wind tunnel and and helicopter-ship trial applications culminating in participation with IDAS. He is now involved with wind tunnel software upgrading, Black Hawk helicopter flight trials for human factor studies, and is responsible for maintenance of the Air Operations Simulation Centre (AOSC) Partial Dome Flight Simulator Display.

S.A.Kent
Air Operations Division

Steven Kent is a Senior Technical Officer who has completed both a Certificate of Technology and an Associate Diploma in Electronics Engineering. He has been employed at the Aeronautical and Maritime Research Laboratory since 1982 and has gained extensive experience in data acquisition and measurement applications for a wide variety of projects. He has worked for the Air Operations Simulation Centre since 1992 and has been involved in the development, construction and maintenance of hardware and software for display systems, simulation cockpits and computer systems used in flight simulation and operational and human factors research.

M.M.Israel
Air Operations Division

Maurice Israel commenced as a trainee Technical Officer in 1970 with the then Army Design Establishment (Department of Army) E.E Laboratory. During this period he worked in several areas, including conducting environmental and durability tests on various military equipment. He graduated from Swinburne Institute of Technology in 1974 with an Electrical/Electronics Engineering Certificate. He joined the then Australian Broadcasting Control Board (ABCB) (Department of Communications (DOC)) in 1975 as a Technical Officer in the Broadcasting Engineering Division, which entailed work associated with development of technical standards for TV Broadcast stations and the introduced 'colour service'. In 1979, he participated as a team with the Canadian DOC in a series of satellite field trials. He became a Senior Technical Officer in 1981 and was involved with RF field propagation measurements/coverage of proposed UHF-TV stations. He joined the then Aeronautical Research Laboratories (ARL) in 1986, working in the Flight Simulation Group and was involved in electronic systems supporting research on flight and visual simulation. This was followed by work in human factors with projects relating to 'night vision' and human performance in military systems. In 1993 he joined the Instrumentation and Trials Group where he was involved in helicopter-ship flight trials for the Australian Navy and facilitated the development of IDAS in 1994. He is currently working in the Air Operations Simulation Centre at the Aeronautical and Maritime Research Laboratory.

Contents

Acronyms

ADC	Analogue to Digital Converter
AMAFTU	Aircraft Maintenance And Flight Trials Unit
AMRL	Aeronautical and Maritime Research Laboratory
AOD	Air Operations Division
AT	Advanced Technology
COM	Communication
CPU	Central Processor Unit
CRT	Cathode Ray Tube
DAC	Digital to Analogue Converter
DARTH	Data Acquisition Real Time Hardware
DC	Direct Current
DMA	Direct Memory Access
DOS	Disk Operating System
DRAM	Dynamic Random Access Memory
EL	Electro Luminescence
EMI	Electro Magnetic Interference
FIFO	First In First Out
FOCFT	First Of Class Flight Trial
I/P	Input
IDAS	Integrated Data Acquisition System
ISA	Industry Standard Association
LCA	Logic Cell Array
LED	Light Emitting Diode
MADAR	Microprocessor Airborne Data Acquisition & Replay
MIL-STD	Military Standard
O/P	Output
PC	Personal Computer
PCI	Peripheral Component Interconnect
PROM	Programmable read Only Memory
RAN	Royal Australian Navy
RS232	Electronic Industries Association bus standard RS232
RS485	Electronic Industries Association bus standard RS485
RTSI	Real-Time System Intergration
SCSI	Small Computer Serial Interface
SHOL	Ship Helicopter Operating Limit
SOR	Statement of Requirement
TTL	Transistor - Transistor Logic
VADAR	Versatile Data Acquisition & Replay
VME	VersaModule Eurocard

1. Introduction

The Integrated Data Acquisition System (IDAS) was developed by the Air Operations Division (AOD) of the Aeronautical and Maritime Research Laboratories (AMRL) to meet the helicopter flight trials requirements of the Aircraft Maintenance and Flight Trials Unit (AMAFTU) of the Royal Australian Navy (RAN). The development was carried out to meet the requirements laid out in a statement of requirement (SOR) provided by AMAFTU, which has been summarised in Appendix 1. AOD has had a long association with AMAFTU, being first involved with the unit in the late 1970s in providing instrumentation to record flight parameters from a Sea King helicopter for the validation of a mathematical model (developed by AOD) of this helicopter. At that time AMAFTU had no data acquisition systems of its own and relied on AOD to provide suitable instrumentation. AOD designed and commissioned a Microprocessor Airborne Data Acquisition and Replay (MADAR) system (Ref. 1) which was operated successfully by AMAFTU for many years for acquisition of data in both helicopters and ships. MADAR was superseded in 1989 by an updated system known as the Versatile Airborne Data Acquisition and Replay (VADAR) system (Ref. 2). VADAR was also used successfully in First of Class Flight Trials (FOCFTs) with the Seahawk and Black Hawk helicopters on various ships. In 1991 VADAR was modified to enhance the versatility of the system, and became the Data Acquisition Real Time Hardware (DARTH) (Ref. 3). Both VADAR and DARTH were designed around economically priced commercially available Personal Computer (PC) Advanced Technology (AT) bus compatible hardware. All the signal processing hardware and software were designed at AOD.

IDAS is an enhanced version of DARTH, featuring faster operation, more versatile hardware, and greatly increased data storage capacity. The main use of these data acquisition systems is for FOCFTs. These trials establish the Ship Helicopter Operating Limits (SHOLs) for various helicopter types operating from RAN ships. Trials of this nature require two time synchronised data acquisition systems to be operated independently. One is installed in the helicopter (for example Navy Squirrel shown in Fig 1a and 1b) to record aircraft attitude and flight controls, the other on the ship to record ship motion and wind vectors.

Both MADAR and VADAR systems were designed to be experimental equipment, and as such do not necessarily comply with military specifications. Generally, economically priced commercial and industrial quality components were used and found to perform reliably.

AOD at the request of the Royal Australian Navy raised a sponsored task (NAV93/199) to assist AMAFTU in designing the IDAS system and $A400,000 was allocated by Navy for the purchase of equipment required for the IDAS. The final cost of equipment was less than $A300,000, saving the Navy over $A100,000.

Figure 1a. IDAS Installed in Navy Squirrel Helicopter

Figure 1b. IDAS Installed in Navy Squirrel Helicopter

2. Description of IDAS

With many years of experience in flight trials, AMAFTU have defined their needs in a Statement of Requirement (SOR) for an IDAS. A summary of this document is as follows:

1. Capture and recording of analogue data from various transducers fitted to aircraft controls. Forty eight differential inputs with input impedance of 1 MΩ and voltage range of +/- 10 V.
2. Capture and recording of synchro or resolver data from up to 16 aircraft ship sources, both 11.8 V and 90 V at 400 Hz.
3. Capture and recording of frequency signals from up to 8 sources (eg rotary anemometers).
4. Capture and recording of selected data from the aircraft Military Standard (MIL-STD) 1553 bus.
5. Ten analogue Outputs (O/Ps) in the range +/-10 V to drive external equipment such as analogue dial gauges.
6. The ability to accept external control input from a handheld Pilot Control Unit (PCU) via an RS232 serial I/O port.
7. The ability to send selected data via an RS485 serial I/O port to a Pilot Display Unit (PDU).
8. The ability to accept data from the ANZAC frigate anemometer via an RS485 serial I/O port.
9. The requirement for four IDAS systems to provide support for AMAFTU trials.

To meet the above requirements AOD, in conjunction with AMAFTU, selected commercially available equipment where possible, developed additional equipment, and produced a total system, as shown in Figure 2. IDAS offers advanced techniques for sampling, converting, and storing data from various sources at variable rates up to 100 Hz. The PC-based IDAS system architecture provides the user with control of the custom-designed signal conditioning daughter and mother boards that plug into the industry standard association (ISA) bus. A user-friendly operator interface is a critical part of the new system, and where possible a Windows-based environment has been implemented. The exception to the Windows environment is the program, which records the data to disk. This needed to be DOS based in order to execute it at the appropriate rates.

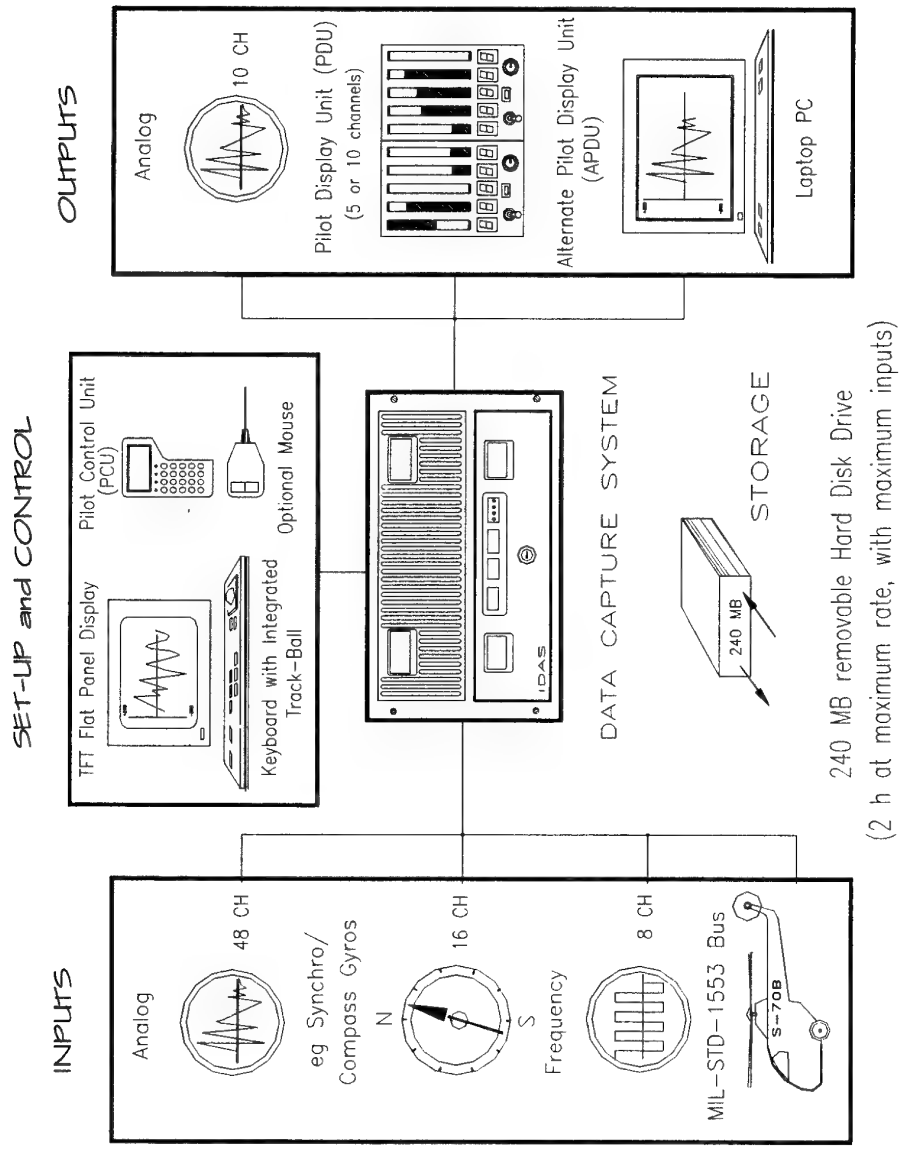

Figure 2. Integrated Data Acquisition System (IDAS) Overview

2.1 General Purpose Industrial PC

The IDAS is based on an industrial PC chassis with a 20-slot ISA passive back plane. The central processing unit (CPU) is a single card Pentuim-90 with 32 Mb random access memory (RAM), on-board hard and floppy disk controllers, plus a small computer system interface (SCSI). The plug-in CPU card can be upgraded as required. The supporting data acquisition hardware is a mixture of commercially available boards and AOD-designed boards. Commercial boards were used where available and AOD-designed boards were only used when no suitable commercial equivalent could be found.

The IDAS is to be fitted into a Navy-built rack for mounting in the helicopter. This rack carries a motion platform (this provides linear and angular data in three axes), the interfacing connections and cables to the aircraft, and two interface boxes. These two AOD-built boxes are the analogue output buffer and the frequency counter signal conditioner.

The features of the industrial PC are:

- the case is a fully enclosed robust design which can withstand 10*g* three axis shock and 1.5*g* three axis vibration, and is suitable for mounting in a standard 19 inch rack. The chassis has a mass of 22 kg and measures 483×267×432 mm;
- the case has forced air cooling (four fans) with filtered air intake;
- the internal air pressure is higher than ambient (positive pressure) to prevent contaminants or particles entering the case;
- there is shielding against electromagnetic interference (EMI); and
- the design is based on a passive backplane rather than a motherboard.

The backplane is a printed circuit board with PC edge connectors and no active components, and is rigidly attached to the bottom of the case. Included in the chassis is a 350 W 'autosense' power supply, and provision for mounting floppy disk, hard disk, and removable hard disk drives (see Appendix 3 for details).

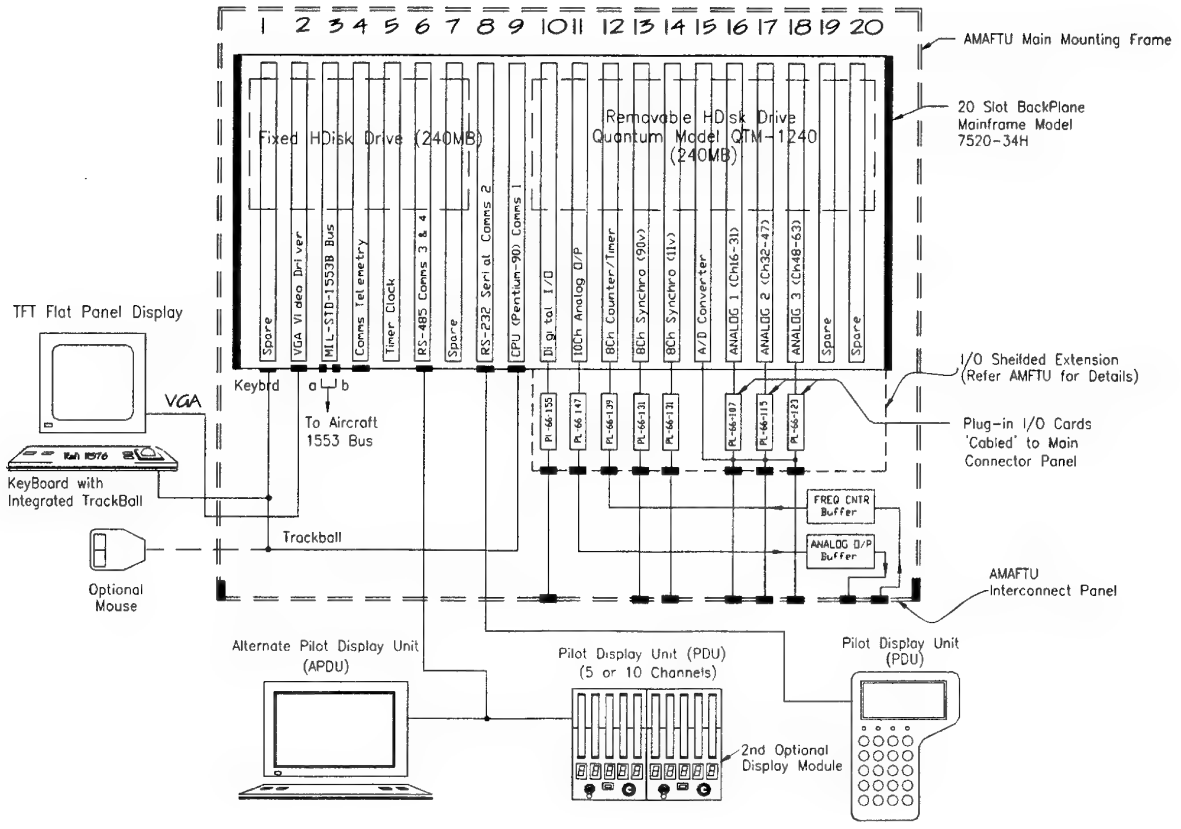

Figure 3. Integrated Data Acquisition System (IDAS) Schematic Diagram

The following list shows the slot allocations for the IDAS (Fig 3). When viewed from the rear, slot 1 is on the left hand side.

Slot 1 spare
Slot 2 Electro Luminescent (EL)/VGA Display Driver Card
Slot 3 MIL-STD-1553 bus Interface Card
Slot 4 RS232 Communication for Telemetry
Slot 5 IDAS Timer Clock Card, type GT401
Slot 6 Serial Communication Board, COM 3 and COM 4, RS485
Slot 7 spare
Slot 8 Serial Communication connector, COM 2
Slot 9 Pentium 90 Processor Card/ Parallel Port / Serial Port, COM1
Slot 10 Digital I/O Card (32 Channel)
Slot 11 Analogue O/P Card (10 Channel)
Slot 12 Frequency Counter Interface Card - Channels 0 - 7
Slot 13 Synchro Interface Card 1 - Channels 0 – 7 (90 V synchro)

Slot 14 Synchro Interface Card 2 - Channels 8 – 15 (11.8 V synchro)
Slot 15 64 Channel Analogue to Digital Converter Card
Slot 16 Analogue Interface Card 1 - Channels 0 -15
Slot 17 Analogue Interface Card 2 - Channels 16 - 31
Slot 18 Analogue Interface Card 3 - Channels 32 - 48
Slot 19 spare
Slot 20 spare

In order to prevent signal reflections on the unusually long ISA bus backplane, an option to install terminating resistors has been provided. The aim of the terminating resistors is to match the impedance of the signal lines and reduce the effect of bus reflections, allowing correct operation of the CPU. The IDAS has either 330 Ω or 220 Ω terminators fitted as per the manufacturer's specification.

2.2 Single Board Computer

Initially the board selected was a single board ISA bus computer with a 486DX2 CPU operating at 66 MHz with 8 Kb of internal cache memory, 32 Mb of dynamic random access memory (DRAM), and on-board hard and floppy disk controllers. This was later replaced with a 90 MHz Pentium board with 32 Mb of DRAM and on-board SCSI controller in an effort to improve system performance.

The SB586TCP/90 is a full-featured ISA bus single board computer. Designed primarily for industrial applications, it is based on the Intel Pentium 90 MHz microprocessor, with included features of :

- 32 Mb of onboard DRAM;
- 256 Kb L2 cache memory;
- 2 Serial, 1 parallel ports;
- IDE, PCI local Bus, and PCI SCSI interface; and
- watchdog timer (not used).

See Appendix 2 for more information.

2.3 AOD designed boards

In general the IDAS input/output signal conditioning requirements could not be met using commercially available ISA bus boards. For this reason, AOD designed a full length programmable ISA bus signal conditioning board known as a "mother board". This card carries up to eight plug-in "daughter boards" (see Fig 4a). Mother boards provide the daughter boards with input and output signals, power and programmable frequency clocks. Through the ISA bus, programming and operation of the daughter cards may be done by software (see Fig 4b).

Bus interfacing requirements have been met by incorporating onto the board a XILINX Logic Cell Array (LCA) (see Fig 4b), which provides enough logic functions to act as the intermediary between the PC/AT bus and the daughter boards.

The LCA is a high density programmable gate array. The array architecture consists of three types of configurable elements: I/O blocks, configurable logic blocks and interconnection networks. On-chip logic provides for automatic loading of configuration data at power-up from the programmable read only memory (PROM) situated on the motherboard.

Three types of daughter boards may be loaded onto a mother board, enabling a single card to perform several interface functions. A fully loaded mother-daughter board combination can provide either sixteen analogue channels, eight synchro channels, or eight frequency measuring channels. Each daughter board can be individually addressed by the PC, which can identify the type and serial number of each board, and the serial number of each mother board.

The standard IDAS configuration has six mother boards fitted, three for analogue signal conditioning, two for synchro to digital conversion and one for frequency measurement.

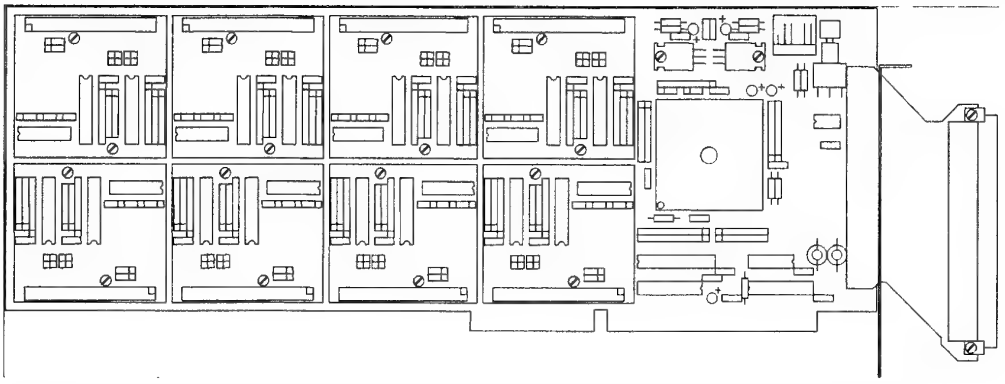

Figure 4a. AOD-Designed PC-AT Mother Board with Eight Daughter Boards

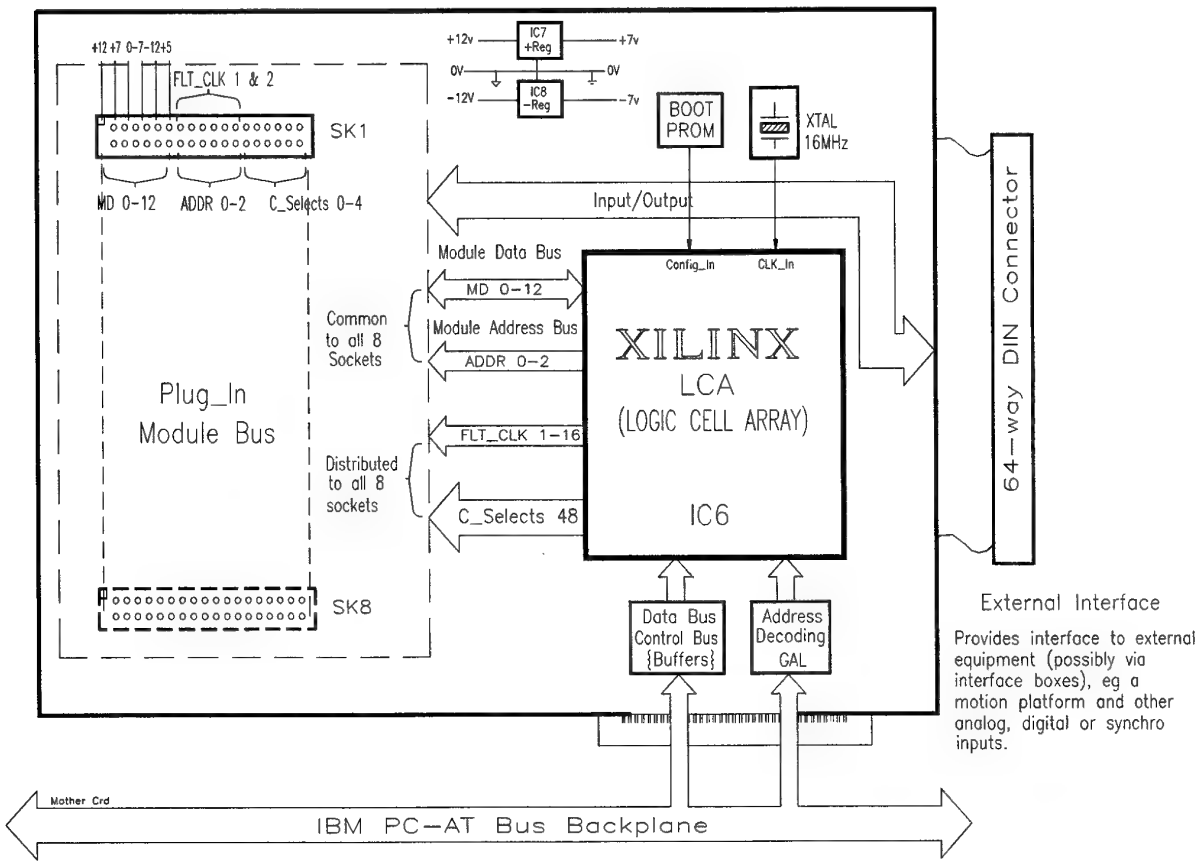

Figure 4b. AOD Designed PC-AT MotherBoard Schematic Diagram

2.3.1 Analogue Input Daughter Board

The analogue signal conditioning daughter boards (Fig 5) have differential inputs and provide three main programmable functions: input offset voltage, gain and low-pass filtering. These functions are all controlled by software via the PC bus. The differential input impedance is 1 MΩ and the input range is ±10 V. A ribbon cable feeds the single-ended output signals from the mother card to the analogue to digital converter card.

An offset in the range ±10 V may be applied by a programmable 12 bit Digital to Analogue Converter (DAC) to each front end amplifier, allowing channel offsets to be zeroed during calibration. User care is needed to distinguish between a voltage offset occurring at the input, that should be zeroed, and a valid signal produced by the installed position of a transducer. For unipolar signals (eg only positive), it may be desirable to deliberately introduce a near full-scale offset to utilise the full 20 V range of the channel.

A programmable gain amplifier gives each channel an overall gain choice of five settings: 0.5, 1, 2, 4, or 8. The final output is a single ended bipolar signal of ±5 V.

The board also includes a fifth order low pass Butterworth switched capacitor filter on each channel. These filters are programmable to provide cut-off frequencies from 1 Hz to 40 Hz, preventing aliasing when sampled at the standard IDAS rates of 100 Hz or less. The signal cut-off frequency depends on the frequency of the clock supplied to the filter by the mother card. It is important that the sample rate selected for an individual channel is at least twice that of the channel cut-off filter frequency to avoid possible aliasing of the recorded channel data. Preferably the sample rate should be greater than five times the channel cut-off frequency for good reconstruction of the original signal waveform. Cut-off frequency and sampling rate are both software selectable.

Whenever an offset voltage exists, there is potential difficulty in later establishing the true zero value from the recorded data, especially if gain changes were involved. To overcome this difficulty, the offset applied to each channel and its gain is recorded to disk in the data header, appearing in the front section of each data file.
Each analogue daughter board occupies a quarter of a mother board, and contains four channels, giving sixteen channels per mother board. The 48 channels required by the IDAS system are provided by three of these boards, which are connected by a common ribbon cable to the analogue to digital converter board.

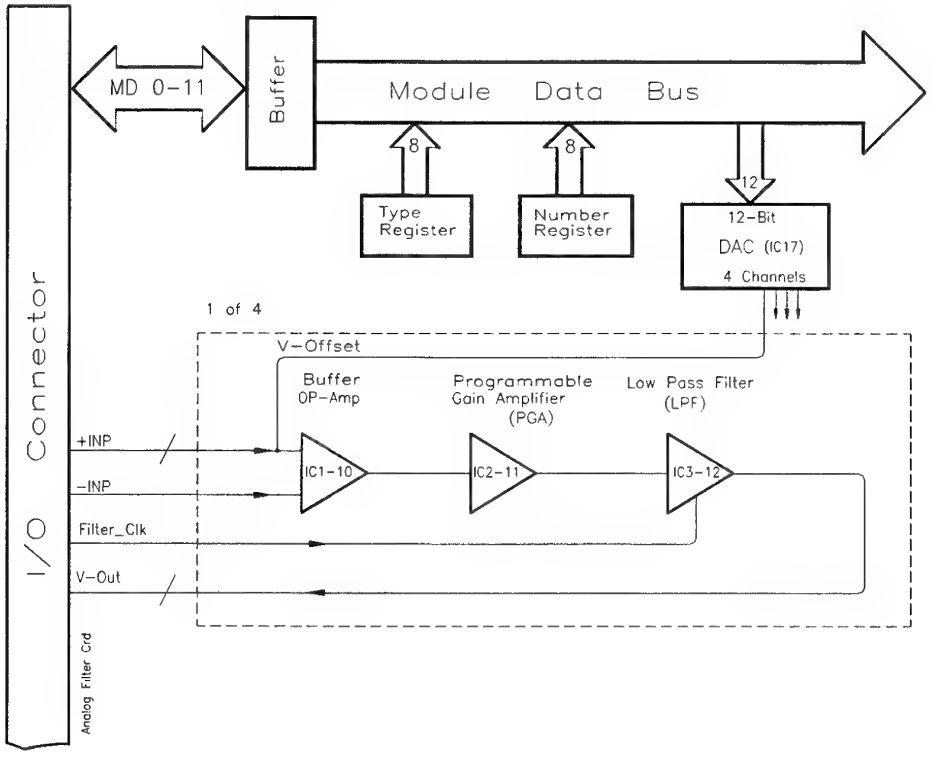

Figure 5. Analogue Input Signal Conditioning Daughter Board

2.3.2 Synchro Input Daughter Board

Resolvers and synchros are rotating transducers, which produce AC electrical signals representing their shaft angular position. Resolvers are four-wire devices and synchros are three-wire devices.

The IDAS synchro daughter board (see Fig 6) is configurable via links to accept either synchro or resolver inputs (synchro by default). An RDC 199220 16-Bit Resolver to Digital Converter chip is the heart of the system, and produces a 16 bit signal which can be read at any time by the PC. The resolution of the converted value is selectable via links to be 10, 12, 14 or 16 bits, and is set to 12 bits by default.

Two standard synchro voltage levels are catered for: 11.8 V and 90 V. The daughter boards are assembled with the resistor network designed to match the intended operating voltage. Eight synchro boards may be fitted to one mother board. Typically, an IDAS system will have six 11.8 V synchros on one mother board, and six 90 V synchros on another mother board, although any combination is possible.

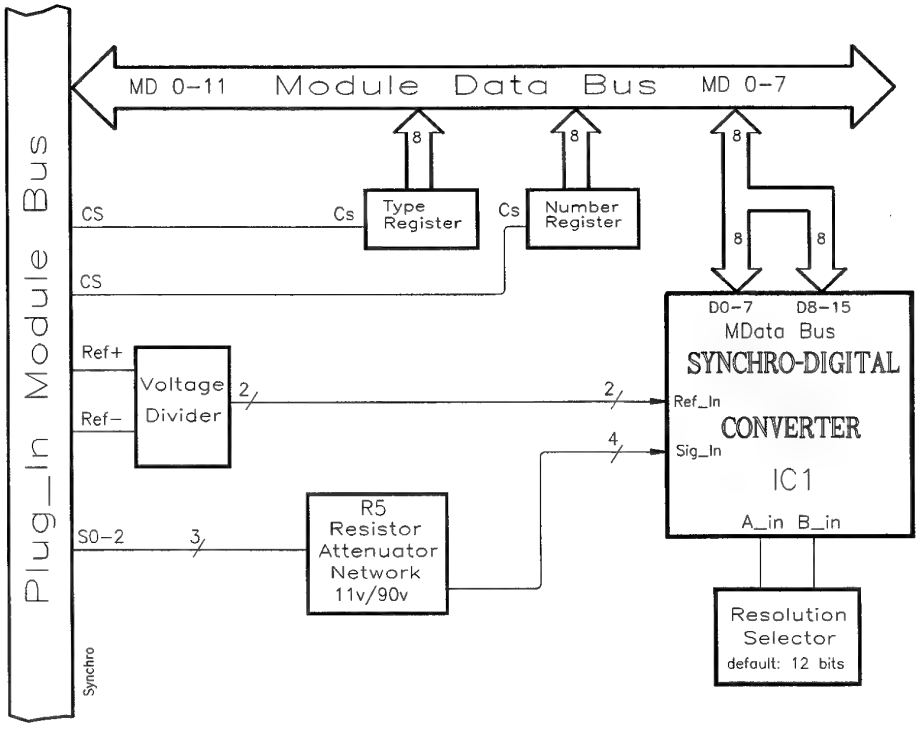

Figure 6. Synchro/Resolver to Digital Converter Daughter Board

2.3.3 Counter/Timer Daughter Board

Signals from transducers such as anemometers (for measuring wind speed and direction aboard ship) produce a periodic signal, the frequency of which varies with propeller rotation. These types of transducers, which can provide pulse or sinusoidal outputs, are fed to an eight-channel signal-conditioning box mounted in the IDAS frame. This box sends a square wave to each of the eight frequency counter daughter boards.

The counter daughter board (see Fig 7) has one main integrated circuit housing three 16 bit counters. These counters are set up to count the pulses from both the input signal and a programmable reference signal supplied by the mother card. The IDAS software compares the two resulting counts, and an accurate measure of the unknown frequency is produced. At least three cycles of the signal are required to obtain a reading; therefore at very low frequencies the update availability is also very low. The minimum frequency that can be measured is 1 Hz, and the maximum frequency is 500 KHz.

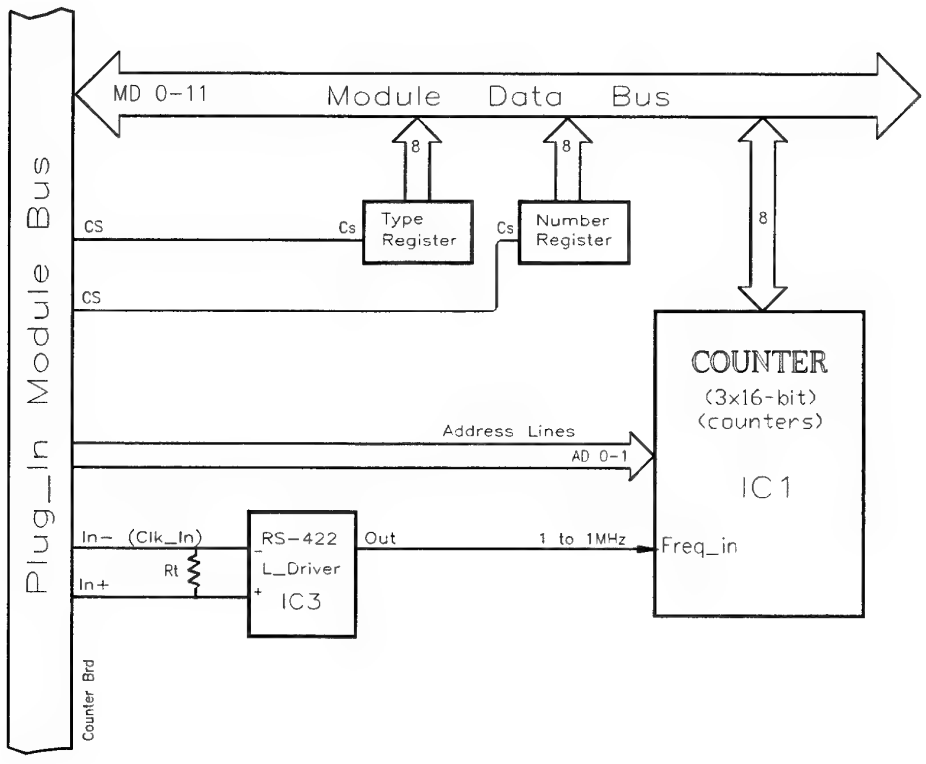

Figure 7. Counter/Timer Daughter Board

2.3.4 Environmental Protection of AOD Designed Boards

AMAFTU recommended that a resilient conformal coating offering environmental protection to components be applied to IDAS circuit boards. This would prevent inadvertent contact with foreign objects that could cause short circuits, and subsequent damage to the aircraft's electronics system. This recommendation was accepted for the AOD designed boards, but was not extended to the commercially obtained boards.
A list of coatings used is shown in Table 1

Table 1. Protective Coatings Used with IDAS Circuit Boards.

Product	Manufacturer	Part No	Supplier	Remarks
'Sylgard' Silicon Elastomer	Dow Corning	Type 182	Farnell Components	Potting/encapsulant
RTV Silicon Rubber	Dow Corning	3140	Farnell Components	Adhesive/sealant
Humiseal Protective Coating	Humiseal Division	Type 1B15H	AMAFTU	Protective Coating Aerosol
Clear Epoxy Lacquer Spray	EPIREZ-Indelab Pty	NA	AMAFTU	Protective Epoxy Coating Aerosol

2.4 Commercial Interface Boards

A number of commercially produced ISA bus boards were used to meet the specifications of IDAS. These include analogue to digital conversion, digital I/O, analogue output, system timing, and MIL-STD-1553 interface.

2.4.1 Analogue to Digital Converter Board

A high-performance 64-channel single-ended analogue input ISA bus board was selected to meet analogue sampling requirements. This board incorporates a fast 12 bit analogue to digital converter capable of sustaining a 200 kilo sample/second rate, with a 5 μs settling time. The input voltage range is ± 5 V with programmable gains of 1, 2, 5, 10, 20, 50, and 100.

The output range of the IDAS analogue signal conditioning circuit was designed to match this board (ie ± 5 V). The gain settings used by the IDAS software are 1 and 2, with higher gains available through the analogue daughter board (1 to 16), resulting in an overall maximum gain of 32. A ribbon connects 48 channels to the IDAS analogue signal conditioning boards, and the software programs the analogue to digital converter (ADC) card to sample only the required channels at rates up to 100 samples/second.

2.4.2 Digital to Analogue Converter Board

This board has 10 high speed 12 bit digital to analogue converters. The outputs may be unipolar or bipolar, and can operate at sample rates up to 200 kHz. A summarised specification for this board is given in Appendix 2. The IDAS software programs this card to use the bipolar ±10 V output mode, and updates any selected channel at a maximum rate of 100 Hz.

2.4.3 RS485 Serial Interface Board

The RS485 board provides a dual channel asynchronous serial communications port, addressed as COM3 and COM4. The card features programmable baud rate, character length, parity and number of stop bits. A summarised specification for this board is given in Appendix 2. The IDAS software uses COM3 to send data to the Pilot Display Unit (PDU) at rates up to 20 Hz. COM4 is used to receive data from the type of anemometer fitted to ANZAC frigates. Wind speed and direction are received five times per second.

2.4.4 Digital Interface Board

This board provides 32 transistor - transistor logic (TTL) digital I/O lines, organised into four 8 bit ports. Each port may be configured as input or output.
The IDAS uses 24 channels as inputs, and 8 as outputs. A summarised specification for this board is given in Appendix 2.

2.4.5 Timer Board and Back-Up Battery

The timing for all events within IDAS is derived from this card, which features a highly accurate real time clock running independently of the PC clock. The card is programmed to generate a PC bus interrupt at 100 Hz, which triggers the sampling of all input sources, updating of outputs, and writing of time-tagged data to disk.

If an accurately set time is to be kept while the IDAS unit is powered down, a backup battery within the IDAS frame will run the real-time clock for 55 hours.

The back-up battery is a rechargeable 5.7 Ah 12 V unit, externally mounted and connected through the board's edge panel. The battery is a sealed lead-acid type with an electrolyte formed from glass cloth impregnated with electrolyte paste between each cell's plates. This construction provides a level of shock protection for airworthiness reasons. Recharging is carried out externally using a proprietary charging unit specially designed for the IDAS timing battery.

2.4.6 MIL-STD-1553 Interface

The MIL-STD-1553 bus is a military standard dual redundant serial bus operating at 1 MHz. The MIL-STD-1553B bus board used in IDAS is the BUS-65517II from Data Device Corporation. It is a full size PC-AT board designed for the test and simulation of MS1553 systems. The BUS-65517II can simultaneously emulate a Bus Controller, multiple Remote Terminals, and/or Bus Monitor, in either MIL-STD-1553 "A" or "B" mode. The on-board stack can accommodate 6 K words which can be read by the PC at any time.

The IDAS software programs the board to monitor and store data from any bus addresses. When required, it may emulate a Remote Terminal and accept control of the bus for short periods to access data not already available.

2.5 Counter-Timer Interface Unit

The counter-timer interface unit is a signal-conditioning unit, which facilitates the connection of a wide variety of periodic signals to the digital input circuit of the counter/timer. The input is a high impedance single ended circuit (see Fig 8a), which rejects DC, and uses a zero crossing detector to produce a square wave (see Fig 8b). This unit is mounted in the equipment rack below the main IDAS chassis and is externally powered from 28 V DC.

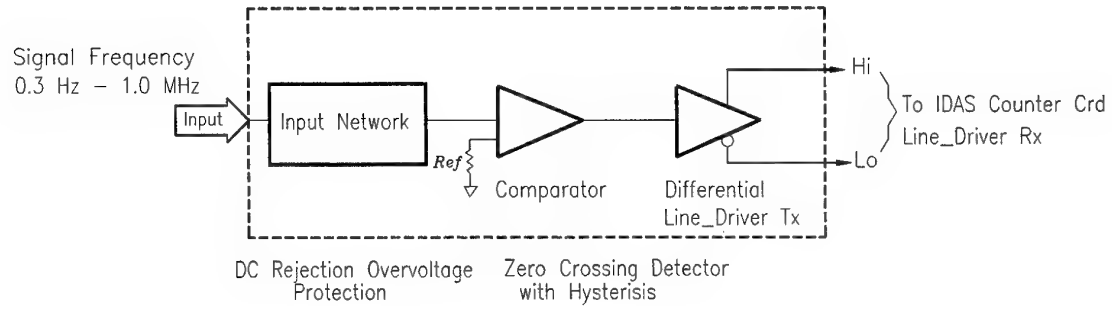

Figure 8a. Block Diagram of Counter-Timer Interface Unit

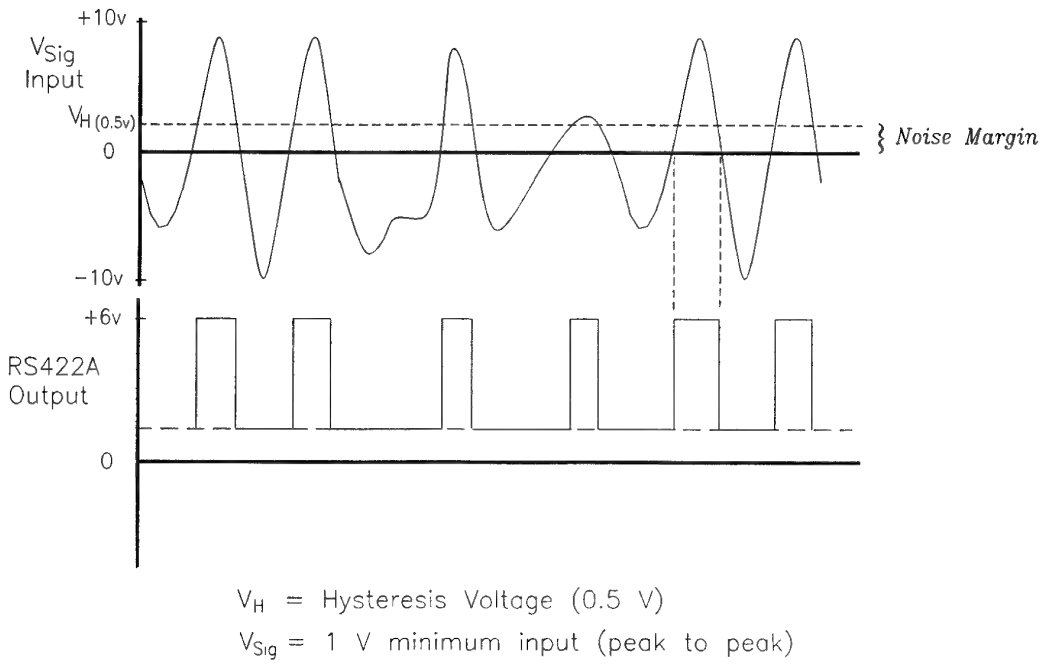

Figure 8b. Typical I/O Signals of Counter-Timer Interface Unit

2.6 Analogue Output Buffer Box

The signals from the analogue output card are passed through the analogue output buffer box to drive AMAFTU's peripheral "Meter Panel". This panel may be used in certain aircraft where the normal IDAS remote display is inappropriate.

The gain and offset controls shown in Fig 9 are screwdriver adjustable controls on the front face of the box. The buffer box is mounted in the equipment rack below the main IDAS chassis.

The unit is housed in a sealed metal box for EMC screening and earthed to the IDAS chassis. The external power supply required is 28 V DC.

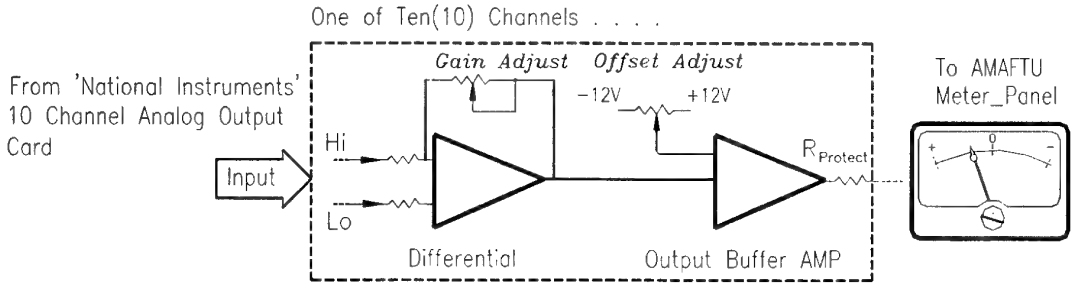

Figure 9. Analogue Output Buffer Amplifier

Each channel is intended to drive a moving coil meter display of typically 75 to 150 Ω resistance, with the gain and offset controls being used to set the calibration for the channel. In addition a series resistance with each output line prevents damage to the unit from inadvertent short circuiting of the output.

2.7 Pilot Control Unit (PCU)

In acquiring data in the helicopter, IDAS is mounted behind the pilot in an enclosed frame. The dangerous nature of some trials requires the IDAS be operated by the copilot to remove any need for a back seat IDAS operator. The pilot is provided with a means of controlling IDAS functions through the PCU.

The PCU is a rugged hand-held control/display unit with alphanumeric and function keys, and a serial RS232 interface. All IDAS keyboard commands are available by typing on the PCU keypad, and four frequently-used commands are programmed into the function keys. The 80 character (4 line × 20) display enables keystroke entries and messages from IDAS to be displayed. See Appendix 3 for the PCU specification.

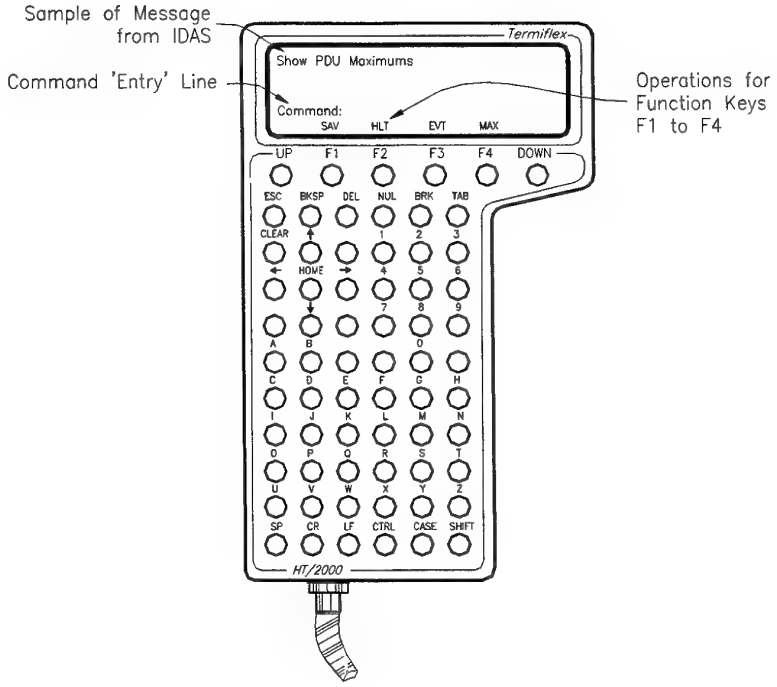

Figure 10. Handheld Pilot Control Unit

2.8 Pilot Display Unit (PDU)

Up to ten of the parameters being monitored by the IDAS may be displayed to the pilot in bar graph form using the PDU. Two types of PDU are available:

- a Notebook PC running a bar graph display program, and;
- a custom made bar graph device known as the Tri Colour LED Display.

The PDU is driven by an RS485 serial communications port from the IDAS chassis, which can control one or both PDUs simultaneously. The graphs are colored green, amber, or red depending on the value displayed, and each graph is configurable in terms of the threshold levels between different colours.

A Notebook PC with a colour VGA screen is the larger of the two options, and may be used in aircraft where enough space is available. The screen can display up to ten graphs, and may be mounted remotely from the body of the PC by a 3 m cable (see Appendix 3 for specifications of the Notebook PC).

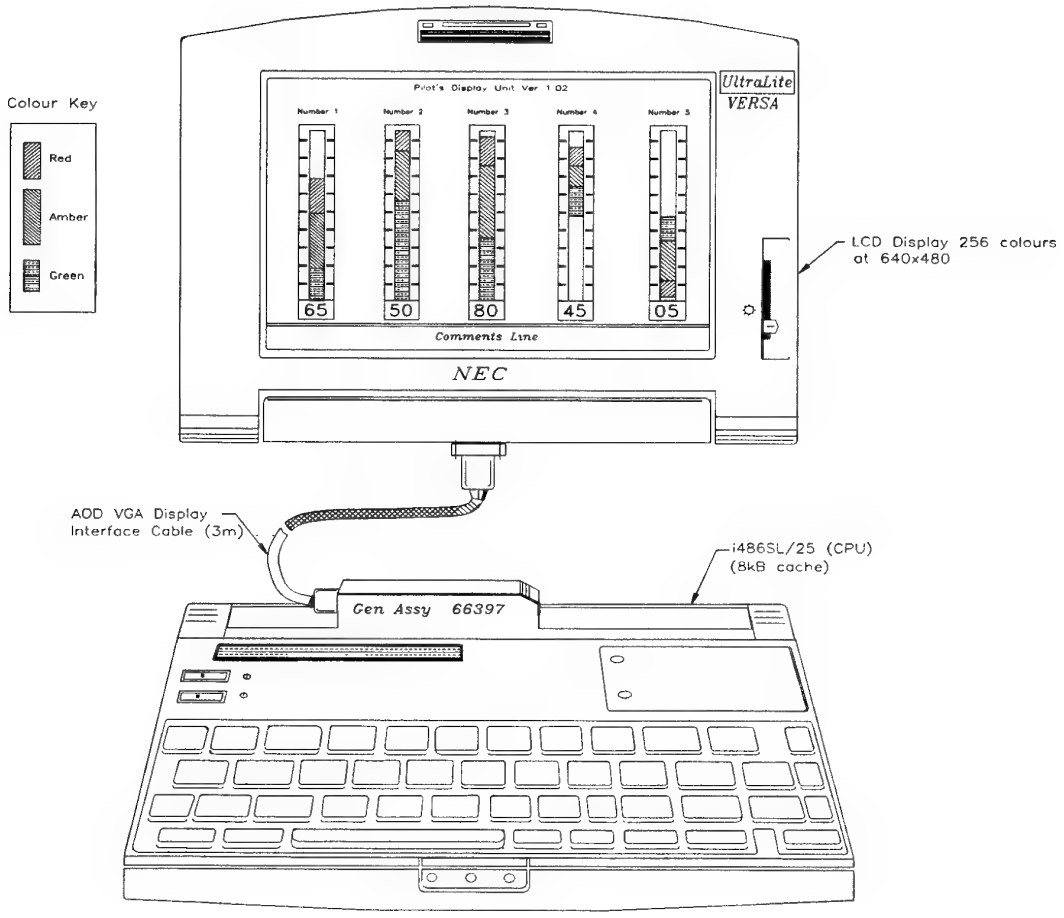

Figure 11a. Pilot Display Unit - Modified NEC Versa Notebook

The AOD-built Tri Colour LED Display is designed to be installed in the console of the Seahawk and to match the existing instrumentation. It has five bar graph displays, and can be expanded to ten by coupling two units together (see Fig 11b and Appendix 3).

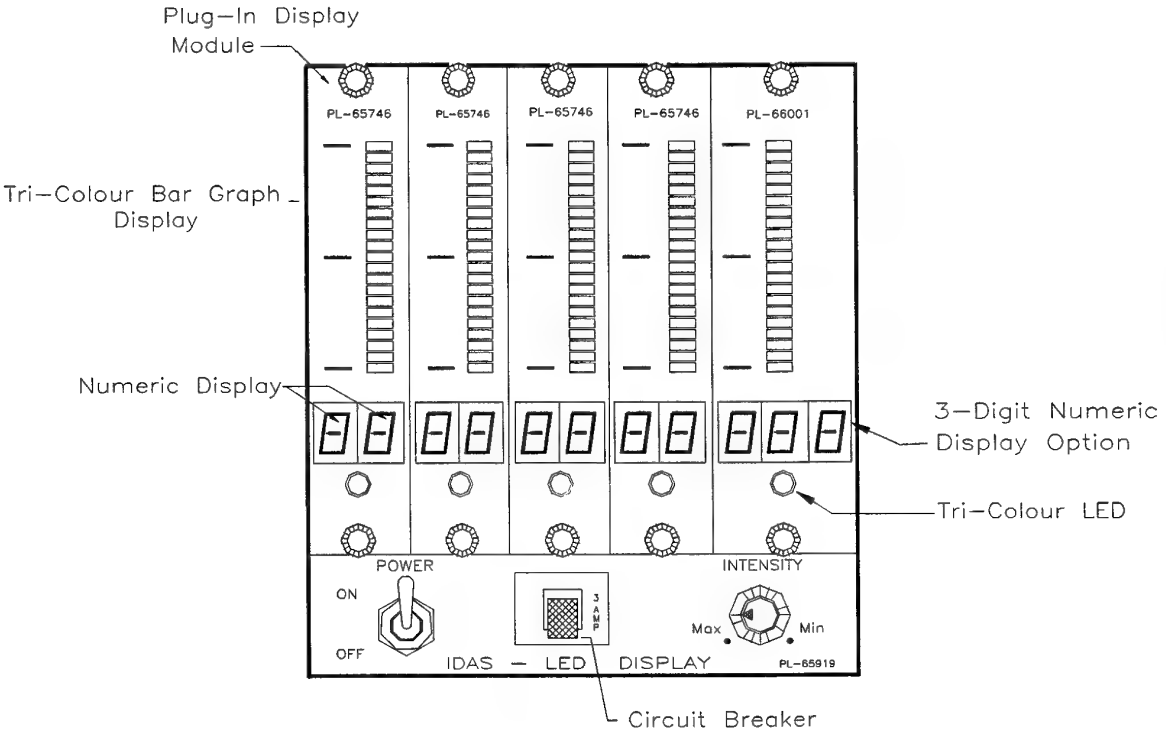

Figure 11b. AOD-designed LED based Pilot Display Unit

Each bar graph may be configured to display any desired parameter. A min/max function controllable from the PCU enables the pilot to view the extreme values reached in the last flight. A separate LED will latch the most extreme colour reached in the last flight (ie if the amber or red zones were entered), allowing a "quick look" at any dangerous parameters.

One major use for the PDU on Seahawk is to inform the pilot of the amount of control authority he has remaining during a difficult landing.

2.9 Display

A VGA compatible flat panel electroluminescent (EL) display was chosen instead of a cathode ray tube (CRT). These displays are rated to operate up to 5000 m above sea level, and are considered safer than CRT type because they do not contain a vacuum and thus cannot implode. Liquid crystal types of flat screen displays are not suitable for this application because their viewing angle is restricted to 40°. The viewing angle of EL displays is a minimum of 160°. The display is fitted with a neutral grey circular polarising filter with anti-reflecting coating.

The EL display is driven by a PC compatible flat panel controller, which can simultaneously provide outputs to both EL and CRT type displays.

2.10 Data Storage

Data can be written during the acquisition phase to the fixed hard disk (240 Mb), and later transferred to the removable hard disk (240 Mb). IDAS is also fitted with a 1.44 Mb 3.5" floppy disk drive.

Recording all available parameters (48 analogue, 16 synchro, 8 frequency, anemometer, selected MIL-STD 1553 bus) at their maximum rates to disk results in usage of over 1.0Mb per minute. The hard disk drive will then provide over three hours of continuous storage.

2.11 Power Supply Modifications

The 300 W Switched-Mode-Power-Supply included with the chassis did not comply with the IDAS SOR. A replacement 'autosense' 350 W power supply from Farnell Advanced Power Ltd in the United Kingdom (UK) was used. The options listed below comply with the requirement:

- increase load current for the ±5 V and ±12 V supply rails;
- provision of "Remote Sensing" of the 5 V output;
- provision of "Power-Fail-Warning" - indicating loss of the main output voltages (not used); and
- provision of an 'autosense' facility for auto-detection of both input line voltage & frequency - this allows connection to either a 115/240 V @ 50/60 Hz or 115/240 V @ 400 Hz power supply.

The standard chassis wiring required upgrading to satisfy the increased current demand of the full complement IDAS system. Fig 12 shows the modified circuit.

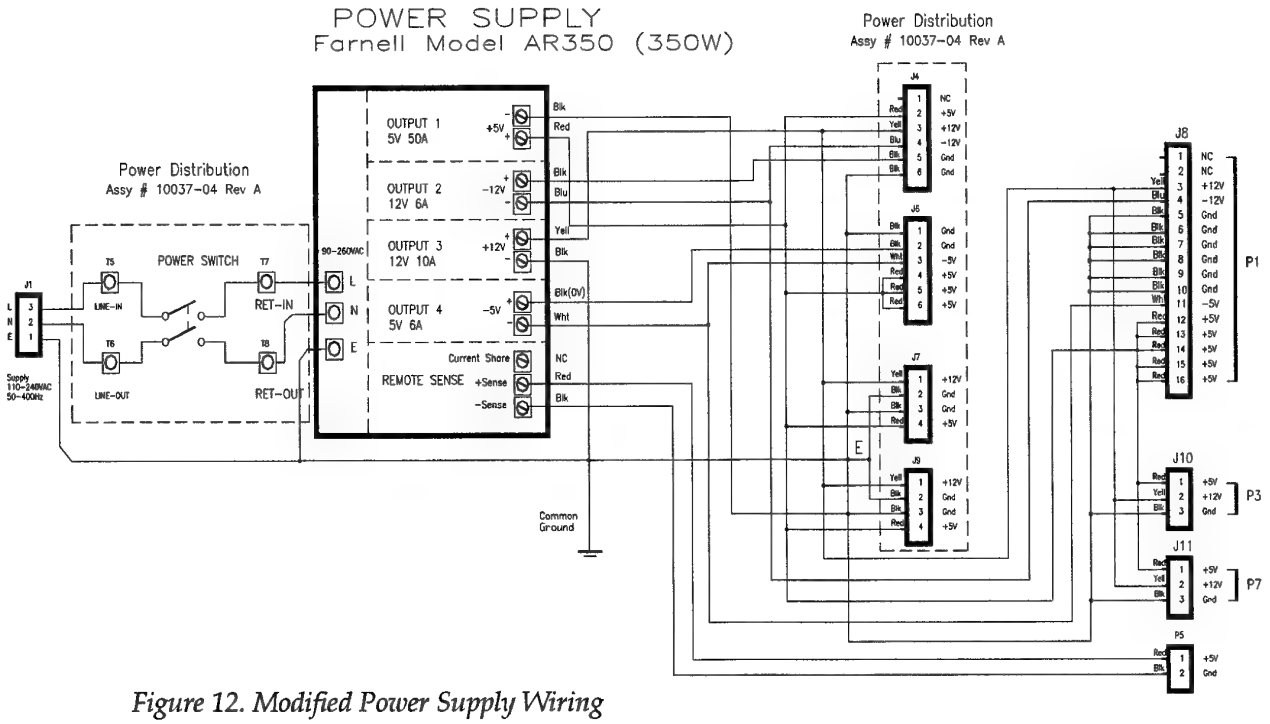

Figure 12. Modified Power Supply Wiring

3. SOFTWARE

3.1 Software Requirements

The IDAS software requirements cover a large area, defining from top-level user interfaces down to implementation details. Some requirements are very specific, but most are general and based on the experience gained when using VADAR.

In addition to the AMAFTU requirements, AOD has requirements on IDAS, since data recorded will frequently be of interest to AOD for validation of mathematical models.

The following software, except where stated, was developed at AOD.

3.11 AMAFTU Requirements

1. Versatility, to meet many different applications without rewriting the software.
2. Ease of use, to avoid extensive training after each round of posting of personnel.
3. Selected information is to be available to the pilot while it is being collected. Such information is to be derived by mathematically processing and combining any or all input data channels.
4. A merge of the data files collected by the two separate IDAS units during a segment of a test must be possible.
5. Software to be divided into separate modules. These modules are Calibration/Setup, Synchronisation, Acquisition, Data Merge, Export/Display, and MIL-STD-1553 bus Data Base entry.

3.12 AOD Requirements

1. Sufficient setup and calibration information is stored in each data file to ensure successful post-processing some considerable time after the data were collected.
2. Raw channel data are recorded rather than partially or fully processed information.

3.2 Approach

The software required by AMAFTU and the IDAS hardware were sufficiently different from that used by VADAR to require the creation of a new set of programs, rather than upgrading the VADAR software. The mixture of data acquisition cards from different suppliers and the highly specialised MIL-STD-1553 card made adapting a commercial data acquisition package to both the AMAFTU and AOD requirements a more daunting task than writing new programs.

The Microsoft Windows environment was chosen as the platform for most of the software modules where significant user interaction was required and no real time data acquisition was involved. The Data Acquisition module was written under Microsoft's Disk Operating System (DOS) using a real-time multitasking kernel to ensure adequate performance under heavy workloads. All programs were written in Microsoft Visual C++ version 1.5.

3.3 Calibration/Setup Program

The purpose of this program is to create or modify a file that defines parameters collected by the data acquisition program. There are three types of parameters: "real" parameters which are directly assigned to an input channel, parameters "derived" from mathematical processing and combination of real data, and "output" parameters to drive output channels.

Drop-down menus allow the selection, naming, and definition of parameters. Attributes defined for a parameter are type (eg analog or synchro), channel number, gain, offset, and sampling rate. A transformation may be applied to a real parameter to convert its raw (and possibly non-linear) value to an engineering unit (eg volts to millimetres of transducer movement). Transformation types available are Boolean, Fifth Order Polynomial, Polynomial Curvefit, Piece-Wise Linear, and Formula. Derived parameters generally take one or more linearised real parameters and apply a Formula (eg sin, cos, sqrt, +, −, ÷, ×) to calculate the desired quantity. For example, large formulas and many inputs are used to obtain Seahawk moving end stop values. Output parameters are linked to specific output channels (eg PDU or analog output), and may use real or derived parameters as their source.

When the source of a real parameter is a MIL-STD-1553 device, the extra information required to specify the address of the device on the Bus is available from a database. A set of dialog boxes enables step-by-step selection.

The program can read data from all the input sources to assist with setting up, but cannot record the data to disk. It can pass data to the PDU, draw graphs and tables on the IDAS VGA screen, and drive the digital and analog outputs.

The calibration of a channel can then be checked by moving a given transducer and monitoring the result in either graphical form on the screen or one of the other output devices.

When all parameters have been calibrated and are working properly, the parameter definition file is saved and the Data Acquisition program may be run. The parameter file will subsequently be used as a header in the data files created by the Data Acquisition program and is shown in Table 2.

Table 2. IDAS Parameter Definition File (also Data File Header) Format

"IDAS"	synchronising characters
"dd/mm/yy hh:mm:ss"	date and time of file creation. *Note: included only in Data file header, not in parameter file.*
"PARA"	signals that parameter definitions are to follow
Version	file format version (only one version exists)
parameter count	number of parameters to follow
"identifier"	first attribute: name of parameter
"units"	second attribute: units
"description"	.
sample rate	.
channel number	.
raw maximum	.
raw minimum	.
.	.
.	.
etc.	(up to 40 attributes)
"identifier"	first attribute of second parameter: name
"units"	second attribute: units
"description"	.
.	.
.	.

3.4 Synchronisation Program

This program enables the IDAS time clocks (not the PC clock) on two independent IDAS units to be synchronised when they are being used in conjunction on a trial. The IDAS unit on the aircraft will be connected briefly via a serial cable to the IDAS unit on the ship, and the clocks synchronised by executing this program on both machines. During the trial, the two IDAS clocks will drift apart, but the error involved may be kept within user-defined limits by re-synchronisation at intervals set by the drift rate. This operational strategy was considered more convenient by AMAFTU than using a global timing source broadcast to both units such as the US GPS.

3.5 Acquisition Program

This program performs all IDAS functions in real time: collecting data from all sources and saving it to disk; calculating all engineering units and derived parameters; driving the PDU and the IDAS graphical or tabular display. The required configuration is read from the parameter definition file (the output from the Setup and Calibration program), and then checked against the IDAS hardware configuration for consistency prior to setting up the hardware as required. Data are acquired and displayed immediately, while the write to disk either starts simultaneously or waits for the pilot or IDAS operator to signal IDAS to "Save". When the required data have been saved, the pilot or operator will signal IDAS to "Halt". The "Halt" does not terminate the program, only the storage of data to disk, and a subsequent "Save" will start writing to a new file. Data files will be distinguished by a name entered or by an automatic name assembled from the time and date the file was created. The data file (Table 3) has two sections: a header followed by the data.

Table 3. IDAS Data File Format

IDAS Header	(see Table 2)
"DATA"	synchronising characters
Length	bytes of data
Timestamp	time of day
Index	record number
Error	not used
data 0	first data word
.	.
.	.
data n	last data word
"DATA"	start of next record
.	.
.	.

The header section of the file is a copy of the parameter definition file created by the Setup and Calibration program. Data are saved in binary form and consist of a time stamp followed by information taken at that particular sample interval. Only raw data, not linearised or transformed data, are saved to disk.

In some cases the Data Acquisition program will have to assume control of the MIL-STD-1553 bus on the Seahawk to acquire data not available by monitoring alone. The main bus controllers provide an opportunity for another system to take over, a feature known as Dynamic Bus Control, and IDAS uses this to retrieve the required data.

3.6 Data Merge Program

The data merge program takes the data files produced by two independent, although synchronised, IDAS units and produces a single data file.

Both header and data sections are combined. This will enable all of the data taken from a FOCFT, both ship and aircraft, to be analysed and archived as a single file. The merged data file will contain all the data, including sections at the start and finish where the times do not overlap.

3.7 Analysis/Export Program

The data analysis program provides AMAFTU with the functions most likely to be used in preparing a SHOL or a report on a trial. It reads the raw data from the disk, evaluates all engineering units and derived parameters, and displays up to six parameters graphically. This display, shown in Fig 13, may be sent to a printer. This program can find exceedances of assigned limits, and any event markers entered by the pilot to indicate crucial time periods (eg landing). Statistics such as mean, median, and standard deviation may be calculated for a selected time slice of a parameter. Sections of the information can be exported to other software packages for further analysis.

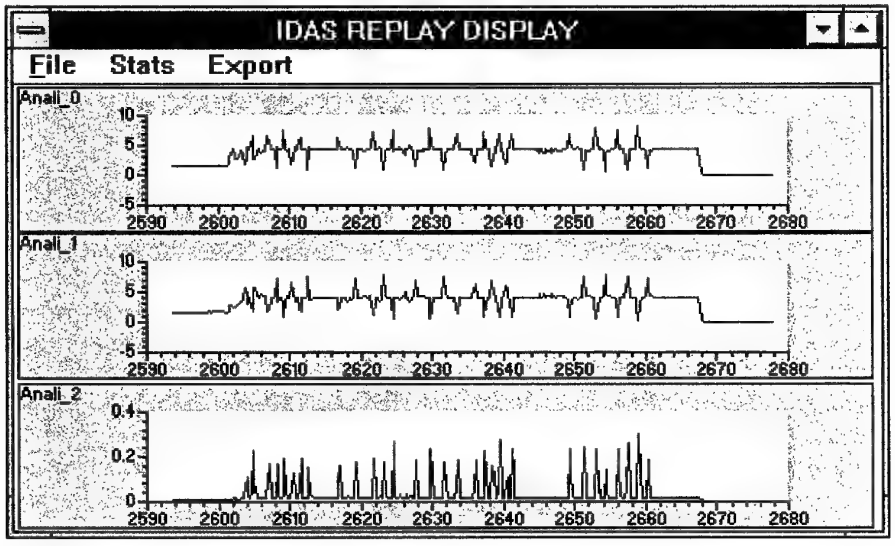

Figure 13. Replay Program Data Plots

The data analysis program is to be augmented by a commercial data analysis and statistics package which will be selected by AMAFTU.

3.8 Pilot's Display Program

Two types of PDUs are provided, each with its own software: the Notebook PC and the LED display.

3.8.1 Notebook Computer Display

The Notebook PC is configured to receive information through its COM1 serial port and display up to ten bar graphs. When powered up, it will automatically run Windows and

execute the PDU program. Configuration information is received when IDAS runs its Data Acquisition program, which gives it the number, style, red/amber threshold levels, and captions of the bar graphs. Data packets are then streamed in and graphs updated 20 times per second

This program was produced by Dr Mike Creek, now at Swinburne University, and subsequently modified by AMAFTU.

3.8.2 Tri Colour LED Display.

This LED-based display system behaves in a way similar to the Notebook to the extent that the IDAS software is not aware which unit it is operating. Both a Notebook PC display and a Tri Colour LED display may be driven at the same time by the same signal. The Tri Colour LED Display software is written in the assembly language of the Motorola 68HC711D3 microcontroller that drives the unit.

3.9 MIL-STD-1553 Bus Data Base Program

The construction and maintenance of databases of MIL-STD-1553 Bus parameters is carried out by a separate program. AMAFTU will enter MIL-STD-1553 Bus information for each aircraft and ship type that will be used in trials. The data-base files created by this program will be read by the Setup and Calibration program to enable the required parameters to be selected and their details entered automatically.

4. CONCLUSION

IDAS is a unique airborne data acquisition system designed to suit the requirements of RAN for helicopter-ship trials. Since flight trials are expensive to conduct, particularly when both ships and aircraft are involved, it is important to ensure that the airborne data acquisition system is reliable, rugged, easily configurable, and simple to operate. The heavy demands upon the pilot's time during a FOCFT require the IDAS be a "start and forget" piece of equipment. Real-time calculations of critical parameters may be displayed in a manner that is easily read to clearly indicate problem situations for both in-flight and post-flight evaluation.

ACKNOWLEDGMENTS

The authors wish to thank the officers of AMAFTU for their assistance in preparing the IDAS Statement of Requirement and construction of the airworthy enclosing frame and aircraft mounts. They also wish to thank the staff of Air Operations Division at AMRL for their effort in design of specialised IDAS hardware and software, in particular, Dr Mike Creek, who has since moved on to the Swinburne University of Technology.

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APPENDIX 1

SPECIFICATION OF IDAS

The IDAS was defined by the RAN's AMAFTU for use in helicopter flight-testing as a replacement for its existing test equipment such as VADAR and DARTH. This appendix is a summary drawn from the statement of requirement provided by the RAN for the IDAS development.

The IDAS was required to be a general purpose aircraft trials data acquisition system optimised for the following applications:

- First of Class Flight Trials;
- development test and evaluation; and
- operational test and evaluation.

A range of data types and sources were required to be recorded as follows:

- analogue voltages - 48 channels with 12 bit resolution;
- synchro - a mixture of 11V and 90 V inputs - 10 channels;
- digital input - 16 single bit input channels;
- frequency – 1 Hz to 1 MHz - 8 channels;
- MIL-STD-1553 - message monitoring and capability for dynamic bus control; and
- RS485 serial - data input through two separate ports.

In addition to recording data from the above inputs, the IDAS was required to control a number of outputs as follows:

- Pilots Display Unit - used to display up to ten parameters either as recorder of after processing (processing may involve multiple inputs and complex formulas) and included marking data limits which were to be displayed by colour changes;
- analogue output - up to 10 output channels required to drive analogue panel meters for displaying parameters to aircrew; and
- digital output - a number of digital outputs were required to indicate processes running in the IDAS, eg event recording.

Control of the IDAS was to be normally done by an operator using a standard PC keyboard with track ball and a VGA electroluminescent screen. However, in some cases a separate operator would not be carried in the aircraft, in which case the pilot must be able to operate the system using a hand-held terminal.

The whole system was to use commercially available components where possible and was to be based on an industrial PC.

An IDAS must be capable of being synchronised with another IDAS and maintain synchronisation over a period of hours with a drift rate less than 10 ms/h.
The data files produced by two separate IDAS's recording over the same period must be capable of being merged into one data file post recording.

APPENDIX 2

COMMERCIAL AT-BUS BOARDS USED IN THE IDAS

In accordance with the SOR, commercially available parts were used where possible. This included many AT-bus compatible boards for data acquisition, communications, and timing functions. A brief description of these boards is given in this appendix.

1. CPU board

The CPU board in IDAS is an SB586TCP/90 single board computer, supplied by Industrial Computer Source, which is designed to operate on a passive backplane.
The board is specified as follows:

Pentium microprocessor at 90 MHz
256 KB write-back cache memory
PCI Local Bus support
PCI SCSI controller
Supports up to 256 MB of on-board DRAM (fitted with 32 MB)
Two serial and one Parallel port
Floppy drive and IDE drive interface
Shadow RAM for System BIOS and peripherals

2. Analogue to Digital Converter Board

This function is performed by a National Instrument AT-MIO-64F-5 High-Speed Multifunction I/O Board for the IBM PC AT with the following characteristics:

Fast 12 Bit ADC - 200 K Sample/s sustained sampling rate
- 64 single ended or 32 differential input channels
- Input amplifier guarantees settling at all gains
- Software selectable range: 0-10 V, ±5 V, ±10 V
- Channels independently programmable gains: 1, 2, 5, 10, 20, 50, and 100 for 10 V range
- 512 sample first in first out (FIFO) ADC buffer
- Internal/external ADC timing and triggering

Two independent double buffered multiplying 12 bit DACs
- two Kwords FIFO DAC buffer

Eight digital I/O lines capable of sinking up to 24 mA each

Three independent 16 bit counter/timers

Software controlled self calibration

RTSI bus for system level timing and multiboard synchronisation.

This card was purchased from National Instruments Australia, PO Box 466, Ringwood, Victoria 3134, Phone (03) 9879 9422, Fax (03) 9879 9179.

3. Analogue Outputs

This function is performed by a National Instruments AT-AO-10 High Performance, 12-bit Analogue Output Board for the IBM PC AT with the following characteristics:

Ten high speed multiplying DACs
12-bit resolution.
Unipolar or Bipolar O/P's available from each DAC
Voltage O/P from each converter
4 to 20 mA current sink to ground from each converter
Onboard reference of 10 V
8 bit digital I/O (configurable in 4-bit ports)
External bipolar reference input for each dual channel pair
Double buffered D/A latches with simultaneous update capability
External update and interrupt signals
DMA and interrupt capability for waveform generation applications
1 Kwords FIFO for continuous throughput
Counter/timer for periodic interrupt or DMA request
Software Calibration
Programmable with LabVIEW software
Typical settling time to within 0.5 LSB of full scale (10 V) within 5 µs.

This card was purchased from National Instruments Australia, PO Box 466, Ringwood, Victoria 3134, Phone (03) 9879 9422, Fax (03) 9879 9179.

4. Digital I/O

This function is performed by a National Instruments AT-DIO-32F high speed digital I/O Board for the IBM PC AT with the following characteristics:

32 TTL digital I/O lines organised into four 8 bit ports
48 mA output drive
Variety of I/O handshaking options for interfacing to almost any peripheral with parallel interface
Dual sets of handshake control lines, each of which can control an independent 8, 16, or 32 bit data transfer
16 bit direct memory access (DMA) with single and dual channel DMA modes
Onboard counters for digital pattern generation
Digital I/O ports can be double or single buffered
Interrupt generation
RTSI bus for system level timing and multiboard synchronisation
Programmable with LabVIEW software.

This card was purchased from National Instruments Australia, PO Box 466, Ringwood, Victoria 3134, Phone (03) 9879 9422, Fax (03) 9879 9179.

5. System Timing

This function is performed by a Guide Technology GT401 Event Timing Controller/monitor Board for the IBM PC AT with the following characteristics:

A high quality 10 MHz oscillator as the time base
Temperature stability +/- 5 ppm 0° to 40° Celsius
Aging < 2 ppm per year or < 0.2 ppm per month
Generates real time in a number of formats
Generates system interrupts
Resolution 0.4 µs
Outputs timing signals via BNC connector
External battery can be used to maintain time when PC is off

6. RS-422/RS-485 Communication Adaptor

This function is performed by a Quadtech DS-200/DS-300 Board for the IBM PC AT with the following characteristics:

Dual channel RS-422 asynchronous communications adaptor
Each channel individually addressable
Each channel can operate a separate system interrupt
16 byte FIFO input and output buffers

APPENDIX 3

IDAS SYSTEM HARDWARE SPECIFICATIONS

1. IDAS Chassis

A ruggedised PC chassis was selected for use with IDAS. Manufactured by Industrial Computer Source, it has the following specification:

19 inch rack mounting case
Dimensions (W, H, D): 483 * 267 * 432 mm
Mass: 21.7 kg
Power Supply: modified from original unit, see 2.11 in main text
Cooling: Four fans, filtered to 0.0003 Micron
Operating Environment:
0 to 50°C, 5 to 95% RH (non - condensing),
10G, three axis shock
1.5G, three axis vibration
to 20,000 ft altitude
Capacity for up to four hard drives
Fitted with a 20 slot passive ISA backplane

2. Pilot Control Unit (PCU)

The PCU selected for use with the IDAS system is the HT 2000, manufactured by Termiflex. This rugged, low power, handheld control and display unit has the following specification:

Four lines * 20 character supertwist LCD display
34 key sealed membrane keypad
RS-232 serial interface
Setup menu to select communications and other parameters
Backlight for LCD display
5 V external power supply

3. Notebook PC used as Pilot Display Unit (PDU)

An NEC "UltraLite Versa" is used as the PDU. The specifications for this notebook PC are as follows:

Intel i486 CPU; 4 MB RAM
256 colour, TFT LCD backlit VGA display
Built in, 83 key QWERTY keyboard
Parallel and serial I/O ports
120 MB hard disk drive
1.44 MB floppy disk drive

4. LED device used as Pilot Display Unit

The LED PDU, which was developed at AMRL, is based on the Motorola MC68HC711D3 high performance microcontroller unit (MCU). It consists of one backplane containing the MCU, serial interface circuits and various peripheral components, and five display boards, each containing the hardware for one channel of data. Two PDUs can be connected together to display ten channels of data simultaneously.

Five display channels per unit, each with:
- 21 rectangular tricolor LEDs, arranged as a bar graph
- One round LED which can act as a 'latch' to record the highest value reached
- seven segment LED numeric display (1 channel has 3 digits, the other 4 have 2 digits) that shows current data value

Serial communication rate: 9600 baud

Display update rate is a maximum of 20 Hz

Power input is a single 28 V supply via a toggle switch and a 3 A resettable circuit breaker

Display intensity controlled by a potentiometer mounted on the front panel

DISTRIBUTION LIST

Integrated Data Acquisition System (IDAS)

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19. ABSTRACT

A data acquisition system based on commercially available personal computer hardware is described. This system was developed to meet the requirements of the Royal Australian Navy in conduct of flight trials with helicopters operating at sea from ships fitted with helicopter flight decks. All aspects of the system are controlled by software, enabling rapid setup of sample rates, gains, and filter characteristics. Data may be displayed in real-time, and further analysis of recorded data performed post-flight.